REMARKS

In the Office Action, the Examiner notes that claims 1, 3-10, 12-14 and 26 are pending and rejected. By this response, Applicant has amended claim 16. No new matter has been entered.

In view of both the amendments presented above and the following discussion, Applicant submits that none of the claims now pending in the application are obvious under the provisions of 35 U.S.C. §103. Thus, Applicant believes that all of the pending claims are now allowable.

It is to be understood that Applicant, by amending the claims, does not acquiesce to the Examiner's characterizations of the art of record or to Applicant's subject matter recited in the pending claims. Further, Applicant is not acquiescing to the Examiner's statements as to the applicability of the art of record to the pending claims by filing the instant responsive amendments.

OBJECTIONS

The Examiner has objected to claim 16 because it is dependent upon canceled claim 15. In response, as suggested by the Examiner, Applicant has amended claim 16 to depend from claim 10. Therefore, the Applicant respectfully requests that the Examiner withdraw the rejection.

REJECTIONS

35 U.S.C. § 103(a)

Claims 1, 3-10, 12-14 and 16

The Examiner rejected claims 1, 3-10, 12-14 and 16 under 35 U.S.C. §103(a) as being unpatentable over the instant application's disclosed prior art in view of Balakrishnan et al. (US 6,611,567, hereinafter "Balakrishnan"). The rejection is respectfully traversed.

The Applicant's disclosed prior art discloses an encoder, including a differential encoder, a constellation mapper, and in-phase and quadrature filters. The Applicant's disclosed prior art, however, fails to teach or suggest Applicant's

invention as a whole. Namely, as acknowledged by the Examiner, Applicant's disclosed prior art fails to teach or suggest at least the claimed limitations of "wherein each VAS comprises a plurality of vector registers (VR) for storing precomputed pulse shaping values and a vector arithmetic unit (VAU) for arithmetically processing a selected vector and an accumulated vector, said selected vector comprising a plurality of pre-computed values selected from said vector registers in response to a received component signal." Furthermore, Balakrishnan falls to bridge the substantial gap as between Applicant's disclosed prior art and Applicant's invention of at least claim 1.

In general, Balakrishnan discloses a method and apparatus for pulse shaping. As taught in Balakrishnan, a set of bits representing a symbol is received and a corresponding output value is generated by adding or subtracting a received coefficient and a received value based on a predetermined one of the set of bits. Balakrishnan, however, fails to teach or suggest Applicant's invention as a whole. Namely, Balakrishnan falls to teach or suggest at least the limitations of "wherein each VAS comprises a plurality of vector registers (VR) for storing precomputed pulse shaping values and a vector arithmetic unit (VAU) for arithmetically processing a selected vector and an accumulated vector, said selected vector comprising a plurality of pre-computed values selected from said vector registers in response to a received component signal."

As taught in Applicant's invention of at least claim 1, the in-phase VAS comprises a plurality of vector registers and a vector arithmetic unit. Similarly, as taught in Applicant's invention of at least claim 1, the quadrature VAS comprises another plurality of vector registers and another vector arithmetic unit. As such, in Applicant's invention of at least claim 1, both the in-phase and quadrature VASs include the components necessary for performing pulse shaping. Furthermore, as evident from Applicant's specification and drawings, the constellation mapper provides in-phase and quadrature signal components to the in-phase VAS and the quadrature VAS, respectively, in parallel. Therefore, according to Applicant's

invention of claim 1, in-phase and quadrature values may be processed in parallel such that pulse shaping is performed in parallel.

By contrast, Balakrishnan discloses that only one value may be processed at a time. In particular, Balakrishnan specifically teaches the use of switches for switching between real and imaginary output values. (Balakrishnan, FIGs. 6, 7, 11). In particular, with respect to FIG. 6, Balakrishnan specifically states that "a first switch 16 receives the output of the add/subtract block 14, and supplies the output of the add/subtract block 14 to either the real or imaginary output of the QPSK processing block QPB...." (Balakrishnan, Col. 4 Line 66 – Col. 5 Line 2; Emphasis added). Similarly, with respect to FIG. 7, Balakrishnan specifically states that "[t]he second switch 24 supplies one of the real and imaginary outputs to the add/subtract block 14, based on the value of the second bit b_1...when the second bit b_1 is 0, the [second] switch 24 supplies the real value...and when the second bit b_1 is 1, the [second] switch 24 supplies the imaginary value...." (Balakrishnan, Col. 6 Lines 13 -63).

In other words, Balakrishnan teaches that a real value is processed and output if the switch is set in the R-position, while an imaginary value is processed and output if the switch is set in the I-position. As taught in Balakrishnan, the switches used for choosing between processing of real and imaginary values may only be set in one position or another. The Balakrishnan switches cannot be set to both the R-position and the I-position simultaneously. As such, real and imaginary values simply cannot be processed in parallel using the Balakrishnan system. Therefore, the teachings of Balakrishnan are completely different from Applicant's invention of at least claim 1.

Furthermore, since only one value at a time (either a real value or an imaginary value) may be processed and output in the Balakrishnan system, Balakrishnan teaches a single coefficient register (illustratively, COEF REG 126 depicted in FIG. 7 of Balakrishnan). Thus, when a switch that alternates between acceptance of real and imaginary values is set in the R-position, the coefficient register provides coefficients for shaping the real value. Similarly, when a switch

that alternates between acceptance of real and imaginary values is set in the I-position, the coefficient register provides coefficients for shaping the imaginary value. Thus, Balakrishnan uses a single coefficient register for processing both the real, as well as the imaginary, values.

In Applicant's invention of at least claim 1, on the other hand, the in-phase VAS comprises a plurality of vector registers for storing precomputed pulse shaping values for shaping the in-phase component. Similarly, in Applicant's invention of at least claim 1, the quadrature VAS comprises a plurality of vector registers for storing pre-computed pulse shaping values for shaping the quadrature component. In other words, as taught in Applicant's invention of at least claim 1, distinct sets of vector registers provide pulse shaping coefficients for the in-phase VAS and the quadrature VAS, respectively. A single coefficient register for serially shaping real and imaginary values, as taught in Balakrishnan, is simply not a first plurality of vector registers having coefficients for shaping in-phase components and a second plurality of vector registers having coefficients for shaping quadrature components such that the in-phase and quadrature pulse shaping is performed in parallel, as taught in the Applicant's invention of at least claim 1.

The teachings of Balakrishnan are completely different from Applicant's invention of at least claim 1. Thus, the design and operation of the Balakrishnan system is completely different from the design and operation of the Applicant's invention of claim 1. As such, Balakrishnan fails to teach or even suggest the Applicant's claimed limitations of "wherein each VAS comprises a plurality of vector registers (VR) for storing precomputed pulse shaping values and a vector arithmetic unit (VAU) for arithmetically processing a selected vector and an accumulated vector, said selected vector comprising a plurality of pre-computed values selected from said vector registers in response to a received component signal." Therefore, Balakrishnan fails to teach or suggest Applicant's invention as a whole.

The test under 35 U.S.C. §103 is not whether an improvement or a use set forth in a patent would have been obvious or non-obvious; rather the test is whether the claimed invention, considered as a whole, would have been obvious. Jones v. Hardy, 110 USPQ 1021, 1024 (Fed. Cir. 1984) (emphasis added). Moreover, the invention as a whole is not restricted to the specific subject matter claimed, but also embraces its properties and the problem it solves. In re Wright, 6 USPQ 2d 1959, 1961 (Fed. Cir. 1988) (emphasis added). Balakrishnan, alone or in combination with Applicant's disclosed prior art, fails to teach or suggest Applicant's invention as a whole.

Furthermore, the Applicant's disclosed prior art and Balakrishnan cannot be operatively combined. The Applicant's disclosed prior art discloses parallel filters for processing the in-phase and quadrature signal components in parallel. As described herein, however, Balakrishnan performs serial processing on real and imaginary values using a plurality of switches for alternating between the real and imaginary values. The Applicant's disclosed prior art expects to receive the in-phase and quadrature signal components in parallel; however, as described above, the Balakrishnan system is only operable for providing real and imaginary values serially using switches that alternate between the real and imaginary values. Therefore, the parallel processing functions of Applicant's disclosed prior art simply cannot be operatively combined with the serial processing functions of Balakrishnan.

As such, Applicant submits that independent claim 1 is non-obvious over Applicant's disclosed prior art in view of Balakrishnan and is patentable under 35 U.S.C. §103(a). Furthermore, Applicant's independent claim 10 recites features similar to the relevant features recited in claim 1. Thus, the Applicant submits that claim 10 is also non-obvious over Applicant's disclosed prior art in view of Balakrishnan and is patentable under 35 U.S.C. §103(a).

Furthermore, claims 3-9, 12-14 and 16 depend, either directly or indirectly, from independent claims 1 and 10 and recite additional features thereof. As such, and for at least the same reasons discussed above, Applicant submits that these

dependent claims are also non-obvious over Applicant's disclosed prior art in view of Balakrishnan and are patentable under 35 U.S.C. §103. Therefore, the Applicant respectfully requests that the rejections be withdrawn.

CONCLUSION

Thus, Applicant submits that none of the claims presently in the application are obvious under the provisions of 35 U.S.C. §103. Consequently, Applicant believes that all of these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Eamon J. Wall, Esq. at (732) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

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